In the Claims

CLAIMS

Claims 1-33 (Canceled).

34. (Currently amended) A transistor assembly comprising:

a plurality of active areas having widths, defined by shallow trench isolation regions, wherein the ~~plurality of active areas have~~ widths of the active areas are no greater than about one micron, and at least some of the widths ~~being~~ are different; and

gate lines disposed over the plurality of active areas to provide individual transistors, those transistors whose widths are different having different threshold voltages from one another.

35. (Original) The transistor assembly of claim 34, wherein the threshold voltages of at least some of the individual transistors are less than one volt.

36. (Original) The transistor assembly of claim 34, wherein individual transistors having active areas with the smaller widths have threshold voltages which are smaller than other individual transistors having active areas with larger widths.

37. (Previously presented) The transistor assembly of claim 34, wherein one of the individual transistors comprises a portion of precharge circuitry for dynamic random access memory circuitry.

38. (Previously presented) The transistor assembly of claim 34, wherein one of the individual transistors comprises a pass transistor.

39. (Previously presented) The transistor assembly of claim 34, wherein one of the individual transistors comprises a portion of sense amplifier circuitry for dynamic random access memory circuitry and has a lower threshold voltage V_{tl}.

40. (Previously presented) The transistor assembly of claim 34, wherein some of the individual transistors are joined together in a parallel configuration.

Claims 41-43 (Canceled).

44. (Previously presented) A transistor assembly comprising:

an active area;

a plurality of spaced-apart shallow trench isolation regions received by the active area and defining active sub-areas therebetween, individual active sub-areas having respective widths, at least one of the widths being no greater than about one micron and at least one other sub-area having a width which is different from the one width; and

a gate line extending over the one and the other sub-area and defining, in part, separate transistors, wherein each of the separate transistors has a different threshold voltage.

45. (Previously presented) The transistor assembly of claim 44, wherein each active sub-area width of an associated transistor is no greater than about one micron.

46. (Previously presented) The transistor assembly of claim 44, wherein each active sub-area width of an associated transistor is no greater than about one micron, wherein more than two separate transistors have different threshold voltages.

47. (Original) The transistor assembly of claim 44, wherein said gate line comprises a common gate line which extends over a plurality of the active sub-areas defining a plurality of transistors, each active sub-area width of an associated transistor being no greater than about one micron.

48. (Original) The transistor assembly of claim 44, wherein said gate line comprises a common gate line which extends over a plurality of the active sub-areas defining a plurality of transistors, each active sub-area width of an associated transistor being no greater than about one micron and said plurality of transistors being joined in a parallel configuration.

49. (Original) A transistor assembly comprising:

an active area;

a plurality of spaced-apart shallow trench isolation regions received by the active area and defining active sub-areas therebetween, individual active sub-areas having respective widths, at least one of the widths being no greater than about one micron and at least one other sub-area having a width which is less than the one width; and

a gate line extending over the one and the other sub-area and defining, in part, separate transistors, wherein the separate transistors have different threshold voltages, wherein said gate line comprises a common gate line which extends over a plurality of the active sub-areas defining a plurality of transistors, each active sub-area width of an associated transistor being no greater than about one micron and said plurality of transistors being joined in a parallel configuration to provide a pull down circuit coupled to a common node.

50. (Previously presented) The transistor assembly of claim 49, further comprising a sense amplifier formed from a pair of transistors, each of the pair having a gate that is cross-coupled to a drain of another of the pair, sources of the pair being coupled to the common node.

51. (Previously presented) The transistor assembly of claim 34, wherein the gate lines are disposed in a direction over the plurality of the active areas, and wherein the widths of the active areas are defined along the direction.

52. (Previously presented) The transistor assembly of claim 44, wherein the gate line extends in a direction over the one and the other sub-area, and wherein the widths of the sub-areas are defined along the direction.

53. (Previously presented) The transistor assembly of claim 49, wherein the gate line extends in a direction over the one and the other sub-area, and wherein the widths of the sub-areas are defined along the direction.

54. (Previously presented) The transistor assembly of claim 49, wherein the parallel configuration comprises an electrical parallel circuit.

55. (Previously presented) The transistor assembly of claim 34, wherein the widths of the plurality of the active areas are less than one micron.

56. (Previously presented) The transistor assembly of claim 44, wherein the respective widths of the individual active sub-areas are less than one micron.

57. (Previously presented) The transistor assembly of claim 49, wherein the respective widths of the individual active sub-areas are less than one micron.

58. (Previously presented) The transistor assembly of claim 34, wherein the individual transistors comprise an electrically parallel circuit configuration.

59. (Previously presented) The transistor assembly of claim 44, wherein the separate transistors comprise an electrically parallel circuit configuration.

60. (Previously presented) The transistor assembly of claim 34, wherein the gate lines comprise a separate and distinct gate line for each of the plurality of the active areas.

61. (Previously presented) The transistor assembly of claim 44, wherein the gate line comprises a separate and distinct gate line for each of the one and the other sub-areas.

62. (Previously presented) The transistor assembly of claim 49, wherein the gate line comprises a separate and distinct gate line for each of the one and the other sub-areas.